APPLICATION FOR UNITED STATES PATENT

FOR

METHOD AND APPARATUS FOR MULTI-ALGORITHM DETECTION

INVENTORS: Perets, Yona
Yellin, Daniel

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Prepared by: Dekel Shiloh

METHOD AND APPARATUS FOR MULTI-ALGORITHM DETECTION

BACKGROUND OF THE INVENTION

[001] A wireless communication device may include a receiver to receive a transmitted signal traveling through a wireless communication channel. The receiver may include a detector to detect symbols of the transmitted signal. The transmitted signal may be affected, e.g., distorted or corrupted, by various types of interference while traveling through the channel. Types of interference may include, for example, white noise, Adjacent-Channel Interference (ACI) or Co-Channel Interference (CCI).

[002] There are detectors using pre-defined detection algorithms intended to improve performance in an environment characterized by white noise interference.

[003] There are also detectors of multiple-antenna receivers using pre-defined detection algorithms intended to improve performance in an environment characterized by CCI.

[004] Detectors using pre-defined detection algorithms may provide sub-optimal results in a dynamically changing environment, e.g., due to movement of a user of the device implementing the algorithm or movement of other users. A relatively small change in the environment, e.g., from an environment characterized by CCI to an environment characterized by white noise interference, may significantly affect the efficiency of the detector since the pre-defined detection algorithm may be sensitive to a particular interference type.

BRIEF DESCRIPTION OF THE DRAWINGS

[005] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with features and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanied drawings in which:

[006] Fig. 1 is a simplified block diagram of a communication system in accordance with some exemplary embodiments of the present invention;

[007] Fig. 2 is a schematic block diagram of a multi-algorithm detector according to some exemplary embodiments of the invention;

[008] Fig. 3 is a simplified, conceptual block diagram of a calculating device in accordance with some exemplary embodiments of the present invention;

[009] Fig. 4 is a schematic flow-chart illustration of a multi-algorithm detection method, according to some exemplary embodiments of the invention;

[0010] Fig. 5 is a schematic block diagram of a dual-algorithm detector according to some exemplary embodiments of the invention; and

[0011]Fig. 6 is a schematic flow-chart of a dual-algorithm detection method according to some exemplary embodiments of the invention.

[0012]It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE INVENTION

[0013]In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However it will be understood by those of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

[0014]Some portions of the detailed description that follows are presented in terms of algorithms and symbolic representations of operations on data bits or binary digital signals within a computer memory. These algorithmic descriptions and representations may be the techniques used by those skilled in the data processing arts to convey the substance of their work to others skilled in the art.

[0015]Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as "processing," "computing," "calculating," "determining," or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices.

[0016]It should be understood that embodiments of the present invention may be used in a variety of applications. Although the scope of the present invention is not limited in this respect, the circuits and techniques disclosed herein may be used in many apparatuses such as receivers of a radio system. Receivers intended to be included within the scope of the present invention include, by a way of example only, cellular radiotelephone receivers, spread spectrum receivers, digital system receivers and the like.

[0017]Types of cellular radiotelephone receivers intended to be within the scope of the present invention include, although not limited to, Code Division Multiple Access (CDMA), CDMA 2000 and wideband CDMA (WCDMA) cellular radiotelephone, receivers for receiving spread spectrum signals, and the like.

[0018]Devices, systems and methods incorporating aspects of embodiments of the invention are also suitable for computer communication network applications, for example, intranet and Internet applications. Embodiments of the invention may be implemented in conjunction with hardware and/or software adapted to interact with a computer communication network, for example, a local area network (LAN), wide area network (WAN), or a global communication network, for example, the Internet.

[0019]Reference is made to Fig. 1, which schematically illustrates an exemplary communication system in accordance with some embodiments of the present invention, enabling a first communication device 100 to communicate with a second communication device 102 over a communication channel 104.

[0020]Although the scope of the present invention is not limited in this respect, communication devices 100, 102 may include wireless modems of computers and communication channel 104 may be part of a WAN or a LAN. For example, the system may be a wireless LAN (WLAN) system. Alternatively, although the scope of the present invention is not limited in this respect, the communication system shown in Fig. 1 may be part of a cellular communication system, with one of communication devices 100, 102 being a base station and the other a mobile station or with both communication devices 100, 102 being mobile stations, a pager communication system, a personal digital assistant (PDA) and a server, etc. In such cases, although the scope of the present invention is in no way limited in this respect, communication device 100 may include a Radio Frequency (RF) antenna 101, and communication device 102 may include an array of m RF antennas 111, as is known in the art. Although the scope of the present invention is not limited in this respect, types of antennas that may be used for antenna 101 and/or antennas 111 may include but are not limited to internal antenna, dipole antenna, omni-directional antenna, a monopole antenna, an end fed antenna, a circularly polarized antenna, a micro-strip antenna, a diversity antenna and the like. In the case of a cellular wireless communication system, according to some embodiments of the invention, the communication system shown in Fig. 1 may be a 3rd Generation Partnership Project (3GPP), such as, for example, Frequency Domain Duplexing (FDD), Global System for Mobile communications (GSM), Wideband Code Division Multiple Access (WCDMA) cellular system and the like.

[0021] Communication device 100 may include a transmitter 106 to transmit a signal, as is known in the art. Communication device 102 may include a receiver 120, which may include a multi-algorithm detector 130, as described in detail below. Receiver 120 may also include an array of m RF to Base-Band (BB) converters 115 to convert RF signals received by antennas 111 into m BB signals 208, as is known in the art.

[0022] In some embodiments, receiver 120 and transmitter 106 may be implemented, for example, using separate and/or integrated units, for example, using a transmitter-receiver or a transceiver.

[0023] Fig. 2 schematically illustrates a block diagram of a multi-algorithm detector 200 according to some exemplary embodiments of the invention.

[0024] According to some embodiments of the invention, detector 200 may be adapted to detect the transmitted signal according to a detection algorithm selected out of two or more detection algorithms based on a pre-selected criterion, as described below.

[0025] According to some embodiments of the invention, detector 200 may receive m input signals 208. Detector 200 may include an array 204 of n sub-detectors 205, wherein n is at least two, and wherein n may be equal to or different than m. Sub-detectors 205 may have inputs associated with at least some of the m signals 208. At least some of sub-detectors 205 may be able, when activated, to detect the transmitted signal, and to provide an output signal 213 including a representation of the detected signal according to a pre-selected detection algorithm, as described below. The pre-selected detection algorithm may include any detection algorithm as is known in the art, for example, a Minimum Mean Square Error (MMSE) algorithm or a Maximal Likelihood Sequence Estimation (MLSE) algorithm, e.g., for example, the algorithm described in US Patent Application 20030123583 to Yellin Daniel et al. Output signals 213 of sub detectors 205 may be provided to a controller 202.

[0026] According to some embodiments of the invention, controller 202 may be adapted to control an output 210 of detector 200 according to pre-selected criteria, as described below. Controller 202 may receive inputs corresponding to at least some of m input signals 208. Controller may also receive inputs corresponding to one or more of n detected signals 213 from sub-detectors 205. In some embodiments, controller 202 may include a calculator 230 to calculate a value, i.e., a Quality Metric (QM), e.g., a Signal to

Noise Ration (SNR), a Log Likelihood Ration (LLR), or a Mean Square Error (MSE), corresponding to signals 208 and signals 213, as described below. Controller 202 may also include a memory unit 231 to store at least some of the values calculated by calculator 230. Controller 202 may further include a max-detector 232 to detect the highest of two or more values, as described below. Max-detector 232 may include any maximum detection algorithm, as is known in the art. Controller 202 may further include a control unit 234 able to control activation of at least some of sub-detectors 205, as described below. Control unit 234 may also control the operation of a selector 206, e.g., by a control signal 216, to connect the output of a selected sub-detector 205 to output 210, as described below. Selector 206 may include any circuitry and/or software to connect the output of the selected sub-detector to output 210. For, example, selector 206 may include a switching device, as is known in the art.

[0027]According to some embodiments of the invention, controller 202 may be able to control activation of one or more of sub-detectors 205 using one or more, respective, control signals 214.

[0028]According to some embodiments of the invention, controller 202 may activate one or more of sub-detectors 205 substantially simultaneously, for example, when controller 202 operates in a "performance" mode of operation, as described in detail below.

[0029]According to other embodiments of the invention, controller 202 may activate one or more of sub-detectors 205 sequentially, for example, when controller 202 operates in a "power" mode of operation, as described in detail below.

[0030]Reference is also made to Fig. 3, which conceptually illustrates a calculating device or unit 300 to perform functions in accordance with some exemplary embodiments of the present invention.

[0031]According to some exemplary embodiments of the invention, one or more of controller 202, calculator 230, max-detector 232, control unit 234, and/or one or more of sub-detectors 205 may be implemented in a unit or a number of units similar to unit 300, which may include a computing unit 310 and a memory 320 coupled to computing unit 310. Although the scope of the present invention is not limited in this respect, computing unit 310 may include an application specific integrated circuit (ASIC), a reduced instruction set circuit (RISC), a digital signal processor (DSP) or a central processing unit

(CPU). The specific type of computing unit 310 and the specific number of units that may be used to implement at least some of the functions described herein may depend on specific implementations and/or design requirements. Instructions to enable computing unit to perform methods according to embodiments of the present invention may be stored in memory 320.

[0032]A QM, e.g., a SNR, a LLR, a MSE or any other suitable QM, as are known in the art, may be calculated for a detected signal, denoted y, provided by a sub-detector, e.g., by one of sub-detectors 205. According to embodiments of the invention, the calculated QM may be used for evaluating performance of the sub-detector providing the detected signal, for example, a higher calculated QM may indicate higher detection efficiency. The QM may vary according to detector-related characteristics, e.g., the detection algorithm used by the sub-detector, and/or according to non-detector related characteristics, e.g., environment-noise characteristics. The QM may be calculated using various calculation methods, as are known in the art. For example, the QM may be calculated according to a pre-decoding method or a post-decoding method, as are known in the art. For example, the QM may be calculated according to the following SNR-related equation:

$$QM = \sum_{i=1}^{l} \left|\hat{h}_c(i)\right|^2 / \left(\frac{1}{N_2 - N_1 + 1} \sum_{j=N_1}^{N_2} \left| y(j) - \hat{h}_c(j) \otimes TSC(j) \right|^2 \right) \quad (1)$$

wherein $y(i)$ denotes the i-th symbol of detected signal y, l denotes the number of symbols per signal, $\hat{h}_c(i)$ denotes a channel estimation tap corresponding to the i-th symbol of y, $TSC(j)$ denotes a j-th symbol of a Training Sequence Code (TSC), and N_1 and N_2 denote first and last indices of the TSC, respectively, as are known in the art. For example, $N1$ and $N2$ may be 1 and 26, respectively, if a pre-decoding method is used, and $N1$ and $N2$ may be 1 and 148, respectively, if a post-decoding method is used.

[0033]Reference is also made to Fig. 4, which schematically illustrates a flow chart of a multi-algorithm detection method, which may be implemented by a multi-algorithm detector, e.g., detector 200, according to some exemplary embodiments of the invention.

[0034]According to exemplary embodiments of the invention, the method may include selecting a mode of operation, e.g., a "performance" mode of operation or a "power" mode of operation, as indicated at block 402. According to some embodiments of the

invention, if the performance mode is selected, a criterion for selecting the detection algorithm may relate to a highest, e.g., a maximal, quality value, e.g., QM, as described below. If the power mode is selected, the criterion for selecting the detection algorithm may relate to a pre-selected minimum quality value, e.g., QM, as described below. According to some embodiments, the modes of operation may be selected manually, e.g., by a user. According to other embodiments, the mode of operation may be selected automatically, e.g., by controller 202. For example, control unit 234 may be able to select between the two modes of operation according to an energy level of a power source, e.g., a battery, used to supply detector 200 with electric energy.

[0035]If the performance mode of operation is selected at block 402, at least some of sub-detectors 205 may be activated substantially simultaneously, as indicated at block 418. For example, control unit 234 may activate, e.g., by signals 214, at least some of sub-detectors 205.

[0036]As indicated at block 420, according to some embodiments of the invention, a QM corresponding to the outputs of activated sub-detectors 205 may be calculated, e.g., by calculator 230, for example, using Equation 1. The QMs calculated by calculator 230 may be stored in memory 231.

[0037]As indicated at block 422, a highest QM of the calculated QMs may be detected, e.g., by max-detector 232, and a sub-detector corresponding to the highest QM may be selected, e.g., by control unit 234.

[0038]As indicated at block 424, the output of the detector may be connected to an output of the selected sub-detector. For example, a selector, e.g., selector 206, may be controlled, e.g., by control signal 216, to connect output 210 to the output of the selected sub-detector.

[0039]If the power mode of operation is selected at block 402, one or more of the sub-detectors may be activated sequentially, e.g., by control unit 234, according to a predetermined activation sequence. For example, as indicated at block 404, a first sub-detector may be activated according to the activation sequence. According to one exemplary embodiment of the invention, the activation sequence may be predetermined according to an estimated performance value of the sub-detectors, e.g., corresponding to previously detected signals. According to another exemplary embodiment of the

invention, the activation sequence may be predetermined according to the robustness level of the sub-detectors, e.g., according to the type and/or number of environments in which the sub-detector is adapted to operate.

[0040]As indicated at block 406, according to some embodiments of the invention, a QM corresponding to the output of the active sub-detector may be calculated, e.g., by calculator 230, for example, using Equation 1.

[0041]As indicated at block 408, the QM of the active sub-detector may be compared, e.g., by control unit 234, with a preset minimum-quality value. The minimum-quality value may be preset according to specific implementations. For example, in a GSM network a minimum-quality value of 100, e.g., corresponding to a 20dB SNR, may be implemented.

[0042]If the QM corresponding to the active sub-detector is equal to or higher than the minimum-quality value, the active sub-detector may be selected, e.g., by controller 202, as indicated at block 410. The output of the detector may be associated with an output of the selected sub-detector, as described above (block 424).

[0043]As indicated at block 412, if the QM corresponding to the active sub-detector is lower than the minimum-quality value, the QM may be stored in a memory, e.g., memory 231. The method may include determining whether a currently activated sub-detector is the last sub-detector, i.e. if a QM has been calculated for all the other sub-detectors. This may be accomplished, for example, by implementing a counter (not shown), as is known in the art, to count the number of QM calculations performed. According to this example, control unit 234 may determine that the currently activated sub detector is the last sub-detector to be activated in the predetermined sequence when a value of the counter equals the number of sub-detectors 205 in array 204.

[0044]If the currently activated sub-detector is determined to be the last sub-detector to be activated in the predetermined sequence, a highest QM of the calculated QMs stored in the memory may be detected, e.g., by max-detector 232. The sub-detector corresponding to the maximal QM may be selected, e.g., by control unit 234, as indicated at block 422. Thus, according to some embodiments, the QM corresponding to the selected sub-detector in the power mode of operation may be lower than the

minimum-quality value, but higher than the QM corresponding to the other sub-detectors 205 in array 204.

[0045] As indicated at block 416, if the currently activated sub-detector is determined not to be the last sub-detector, the active sub-detector may store at least some values, e.g., $y(i)$ and/or $\hat{h}_c(i)$, calculated by the active sub-detector, the active sub-detector may be de-activated, e.g., by control unit 234, and the next sub-detector 205 according to the activation sequence may be activated, e.g., by control unit 234. The QM corresponding to the newly activated detector may be calculated, e.g., by calculator 230, as described above (block 406).

[0046] Reference is made to Fig. 5, which schematically illustrates a block diagram of a dual-algorithm detector 500 according to some exemplary embodiments of the invention.

[0047] According to some exemplary embodiments of the invention, detector 500 may receive a first input signal 518 from a first RF to BB converter 517, and a second input signal 519 from a second RF to BB converter 520. Detector 500 may include a Dual Input Single Output (DISO) MLSE detector 504, a DISO MMSE detector 506, and a DISO selector 508, as are known in the art. MLSE detector 504 may be efficient for an environment characterized by white noise, and MMSE detector 506 may be efficient for an environment characterized by an interference created predominantly by one or more interferers. Detector 500 may also include a controller 502 to control an output 524 of detector 500 according to predetermined criteria, as described below.

[0048] Controller 502 may include a calculator 530 to calculate a QM corresponding to an output of detector 504 or an output of detector 506. For example, calculator 534 may implement Equation 1 to calculate the QM. Controller 502 may also include a memory unit 531 to store at least some values calculated by calculator 230. Controller 502 may further include a max-detector 532, e.g., as described above. Detector 502 may further include a control unit 534 able to control activation of at least one of detectors 504 and 506, as described below. Unit 534 may also control selector 506, e.g., by a control signal 510, to connect output 524 to an output of one of detectors 504 and 506, as described below.

[0049]Reference is also made to Fig. 6, which schematically illustrates a flow chart of a dual-algorithm detection method, which may be implemented by detector 500, according to some exemplary embodiments of the invention.

[0050]According to some exemplary embodiments of the invention, a mode of operation, e.g., a performance mode of operation or a power mode of operation, may be selected, as indicated at block 602. According to some embodiments, the mode of operation may be selected manually, e.g., by a user. According to other embodiments, the mode of operation may be selected automatically, e.g., by control unit 534. For example, control unit 534 may be able to select between the two modes of operation according to an energy level of a power source, e.g., a battery, used to supply detector 500 with electric energy.

[0051]If the performance mode of operation is selected at block 602, control unit 534 may activate detectors 504 and 506 substantially simultaneously, e.g., by signals 514 and 516, respectively, as indicated at block 618.

[0052]As indicated at block 620, according to some embodiments of the invention, calculator 530 may calculate two QMs corresponding to outputs 544 and 546 of detectors 504 and 506, respectively. The QMs calculated by calculator 530 may be stored in memory 531.

[0053]As indicated at block 622, max-detector 532 may detect a highest QM of the QMs corresponding to detectors 504 and 506, respectively. Control unit 534 may select from detectors 504 and 506 the detector corresponding to the maximal QM.

[0054]As indicated at block 624, control unit 534 may control the operation of selector 508, e.g., by control signal 510, to connect output 524 to an output of the selected detector.

[0055]If the power mode of operation is selected at block 602, control unit 534 may activate one of detectors 504 and 506, the detector to be activated may be predetermined, e.g., as described above. For example, detector 504 may be activated, e.g., by signal 514, as indicated at block 604.

[0056]As indicated at block 606, according to some embodiments of the invention, calculator 530 may calculate a QM, e.g., according to Equation 1, corresponding to the output of the active detector, e.g., detector 504.

[0057]As indicated at block 608, control unit 534 may compare the QM of the active detector, e.g., detector 504, with a preset minimum-quality value. The minimum-quality value may be preset according to specific implementations of detector 500, e.g., as described above with reference to block 408.

[0058]If the QM of the active detector, e.g., detector 504, is equal to or higher than the minimum-quality value, control unit 534 may select the active detector, e.g., detector 504, as indicated at block 610. Control unit 534 may control selector 508, e.g., using control signal 510, to associate output 524 with the output of the selected detector, as indicated at block 624.

[0059]As indicated at block 612, if the QM of the active detector, e.g., detector 504, is lower than the minimum-quality value, control unit 534 may store the QM corresponding to the active detector in memory 531. Control unit 534 may also activate the un-active detector, e.g., detector 506, e.g., by signal 516.

[0060]As indicated at block 614, calculator 530 may calculate a QM, e.g., according to Equation 1, corresponding to the output of detector 506. Max-detector 532 may detect a highest QM of the calculated QMs corresponding to detectors 504 and 506, respectively, as indicated at block 622.

[0061]It will be appreciated by persons skilled in the art that the multi-algorithm detectors described above have a significantly improved detection ability in a changing environment, compared to the detection ability of prior art detectors under comparable operational conditions. For example, Spatial Interference Cancellation (SIC) detection methods, as are known in the art, may have relatively optimal performance in environments characterized by an interference of one dominant interferer arriving from a different location than the signal to be detected. However, SIC methods may have relatively sub-optimal performance in environments characterized by an interference of a multiplicity of interference sources positioned in different locations. The multi-algorithm detector, according to embodiments of the invention, may provide relatively optimal performance in different environment types, e.g., the environments described above, by utilizing a multiplicity of multiple-antenna detection algorithms.

[0062]Embodiments of the present invention may be implemented by software, by hardware, or by any combination of software and/or hardware as may be suitable for

specific applications or in accordance with specific design requirements. Embodiments of the present invention may include units and sub-units, which may be separate of each other or combined together, in whole or in part, and may be implemented using specific, multi-purpose or general processors, or devices as are known in the art. Some embodiments of the present invention may include buffers, registers, storage units and/or memory units, for temporary or long-term storage of data and/or in order to facilitate the operation of a specific embodiment.

[0063] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents may occur to those of ordinary skill in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.